

Application No.: 09/653,281

Docket No.: M4065.0278/P278

oxide layer, and a second oxide layer over said nitride layer, said second oxide layer grown by oxidizing said nitride layer with a gas ambient containing atomic oxygen, wherein said second oxide layer is formed to have a thickness of at least 60% of the targeted thickness of the second oxide layer;

*C1 could*  
forming a second conductor layer over said insulating layer;

etching at least said first conductor layer, said second conductor layer and said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in said substrate on an opposite side of said stacked gate structure, thereby forming at least one memory cell.

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16. (Twice amended) A method of forming an ONO insulating structure, comprising:

*C2*  
depositing a first oxide layer over an integrated circuit structure;

depositing a nitride layer over said first oxide layer; and

growing a second oxide layer over said nitride layer wherein said second oxide layer is grown at a temperature of about 850°C to about 1100°C, for about 1 second to about 10 minutes, using a gas ambient containing atomic oxygen.

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31. (Twice amended) A method of forming a flash memory array containing a plurality of flash memory cells, each of said plurality of flash memory cells being formed by the acts of:

*C34 could*  
forming a tunnel oxide on a substrate;

forming a first conductor layer over said tunnel oxide;

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*c3 could*

forming an insulating layer over said first conductor layer, said insulating layer comprising a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer, wherein said second oxide layer is grown in the presence of atomic oxygen at a temperature of less than about 900°C;

forming a second conductor layer over said insulating layer;

etching at least said first conductor layer, said second conductor layer and said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in said substrate, thereby forming at least one memory cell.

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